REMARKS

This is a full and timely response to the outstanding Action mailed March 29, 2004. Upon entry of the amendments in this response, claims 15 - 36 remain pending. In particular, Applicant has added new claims 15 - 36, and has canceled claims 1 - 14 without prejudice, waiver, or disclaimer. Applicant has canceled claims 1 - 14 merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicant reserves the right to pursue the subject matter of these canceled claims in a continuing application, if Applicant so chooses, and does not intend to dedicate the canceled subject matter to the public. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections under 35 U.S.C. 102

The Office Action indicates that claims 1 - 14 stand rejected under 35 U.S.C 102(e) as being anticipated by *Huang* (U.S. 6,117,725). As set forth above, Applicant has canceled claims 1 - 14 without prejudice, waiver, or disclaimer, and respectfully asserts that the rejection has been rendered moot.

Newly Added Claims

Upon entry of the amendments in this response, Applicant has added claims 15 - 36. Applicant respectfully asserts that no new matter has been added. Specifically, support for the limitations recited in new independent claims 15 and 26 can be found, for example, at Figs. 10-13. Applicant respectfully asserts that the pending claims are in condition for allowance for at least the reasons set forth below.

Turning to *Huang*, *Huang* discloses a method of forming an embedded DRAM structure. Specifically referring to Fig. 1, a FET having a gate oxide (14) and a polysilicon gate (16) in logic region (L) and another FET having a gate oxide (14') and a polycide gate (16') are formed on a substrate (10). A first ILD layer (20) is formed covering the FETs. Tungsten plugs (21) electrically connecting to the FETs are formed in the ILD layer (20). Metal lines (22) are formed on the ILD layer (20). A spacer (26) and a Si_3N_4 cap layer (24) are formed to enclose each metal line (22). Referring to Fig. 2, a second ILD layer (28) is formed over the first ILD layer (20). Openings (4) are formed in the second ILD layer (28) in the DRAM region (M). In Fig. 3, metal plugs (30) serving as capacitor bottom electrodes are formed in the openings (4) in the DRAM region (M). With reference to Fig. 4, recesses (8) around the capacitor bottom electrodes (30) are formed in the openings (4). Referring to Figs. 5 and 6, a conformal capacitor dielectric layer (32) is formed over the capacitor bottom electrodes (30). Then, referring to Fig. 7, a capacitor top electrode (34) is formed over the capacitor dielectric layer (32). This is in direct contrast to the features/limitations recited in Applicant's newly added claims.

In this regard, claim 15 recites:

> 15. A method of forming a semiconductor device, comprising the steps of:
> forming at least one first transistor and at least one second transistor in an insulating layer on a semiconductor substrate, wherein the first transistor comprises a first gate and a first gate dielectric layer, and ***the second transistor comprises a dummy gate structure;***
> ***removing the dummy gate structure to form an opening exposing the semiconductor substrate;***
> ***forming a conformal second gate dielectric layer on interior and bottom surfaces of the opening; and***
> ***forming a second gate on the second gate dielectric layer to fill the opening.***

(*Emphasis Added*).

Applicant respectfully asserts that *Huang* is legally deficient for the purpose of rejecting claim 15, because at least the features/limitations emphasized above are not taught or reasonably suggested by *Huang*. Specifically, *Huang* does not disclose "removing the dummy gate structure to form an opening exposing the semiconductor substrate," "forming a conformal second gate dielectric layer on interior and bottom surfaces of the opening," and "forming a second gate on the second gate dielectric layer to fill the opening." Therefore, Applicant respectfully asserts that claim 15 is in condition for allowance. Since claims 16 – 25 are dependent claims that incorporate all the features/limitations of claim 15, Applicant respectfully asserts that these claims also are in condition for allowance. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability.

With respect to claim 26, that claim recites:

> 26. An integrated process of forming a high-voltage transistor and a low-voltage transistor, comprising the steps of:
>
> forming at least one first transistor and at least one second transistor in an insulating layer on a semiconductor substrate, ***wherein the first transistor comprises a high-voltage gate and a first gate dielectric layer, and the second transistor comprises a dummy gate structure;***
> ***removing the dummy gate structure to form an opening exposing the semiconductor substrate;***
> ***forming a conformal second gate dielectric layer on interior and bottom surfaces of the opening; and***
> ***forming a low-voltage gate on the second gate dielectric layer to fill the opening.***

(*Emphasis Added*).

Applicant respectfully asserts that *Huang* is legally deficient for the purpose of rejecting claim 15, because at least the features/limitations emphasized above are not taught or reasonably suggested by *Huang*. Therefore, Applicant respectfully asserts that claim 26 is in condition for

allowance. Since claims 27 – 36 are dependent claims that incorporate all the features/limitations of claim 26, Applicant respectfully asserts that these claims also are in condition for allowance. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability.

Cited Art Made of Record

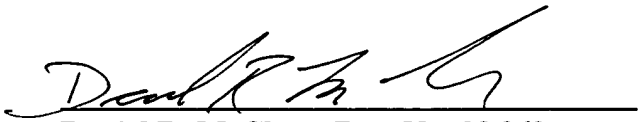
The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action other than those already included herein. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,



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